



La Sapienza

Università degli Studi di Roma

Dipartimento di Informatica e Sistemistica



CALCOLATORI ELETTRONICI

Esame del 15/07/2008 – Soluzione esercizi



Quesito 1 – Tabella di verità

x_4	x_3	x_2	x_1	x_0	N	f
0	0	0	0	0	0	1
0	0	0	0	1	1	1
0	0	0	1	0	2	1
0	0	0	1	1	3	1
0	0	1	0	0	4	0
0	0	1	0	1	5	1
0	0	1	1	0	6	0
0	0	1	1	1	7	0
0	1	0	0	0	8	1
0	1	0	0	1	9	0
0	1	0	1	0	10	0
0	1	0	1	1	11	0
0	1	1	0	0	12	0
0	1	1	0	1	13	1
0	1	1	1	0	14	0
0	1	1	1	1	15	0

x_4	x_3	x_2	x_1	x_0	N	f
1	0	0	0	0	16	0
1	0	0	0	1	17	0
1	0	0	1	0	18	0
1	0	0	1	1	19	0
1	0	1	0	0	20	0
1	0	1	0	1	21	-
1	0	1	1	0	22	-
1	0	1	1	1	23	-
1	1	0	0	0	24	-
1	1	0	0	1	25	-
1	1	0	1	0	26	-
1	1	0	1	1	27	-
1	1	1	0	0	28	-
1	1	1	0	1	29	-
1	1	1	1	0	30	-
1	1	1	1	1	31	-



Quesito 1 – Mappa di Karnaugh – Soluzione A

$x_3 x_2$ \ $x_1 x_0$	00	01	11	10
00	1	1	1	1
01	0	1	0	0
11	0	1	0	0
10	1	0	0	0

$x_2 x_3$ \ $x_1 x_0$	00	01	11	10
00	0	0	0	0
01	0	-	-	-
11	-	-	-	-
10	-	-	-	-

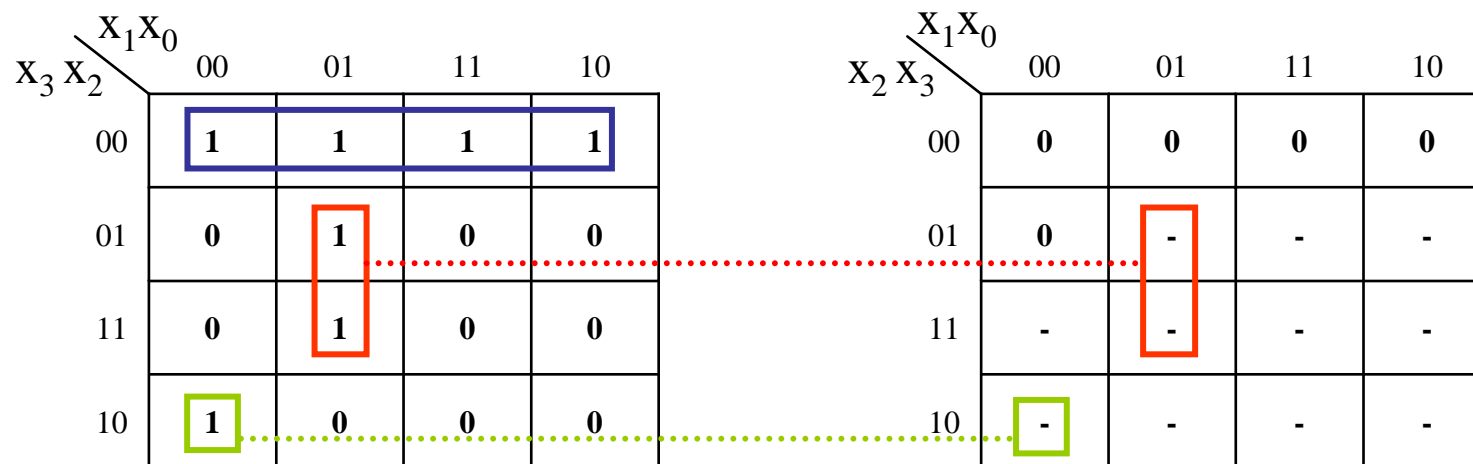
$$x_4 = 0$$

$$x_4 = 1$$

$$f = \overline{x_4} \overline{x_3} \overline{x_2} + x_2 \overline{x_1} x_0 + \overline{x_4} x_2 x_1 x_0$$



Quesito 1 – Mappa di Karnaugh – Soluzione B



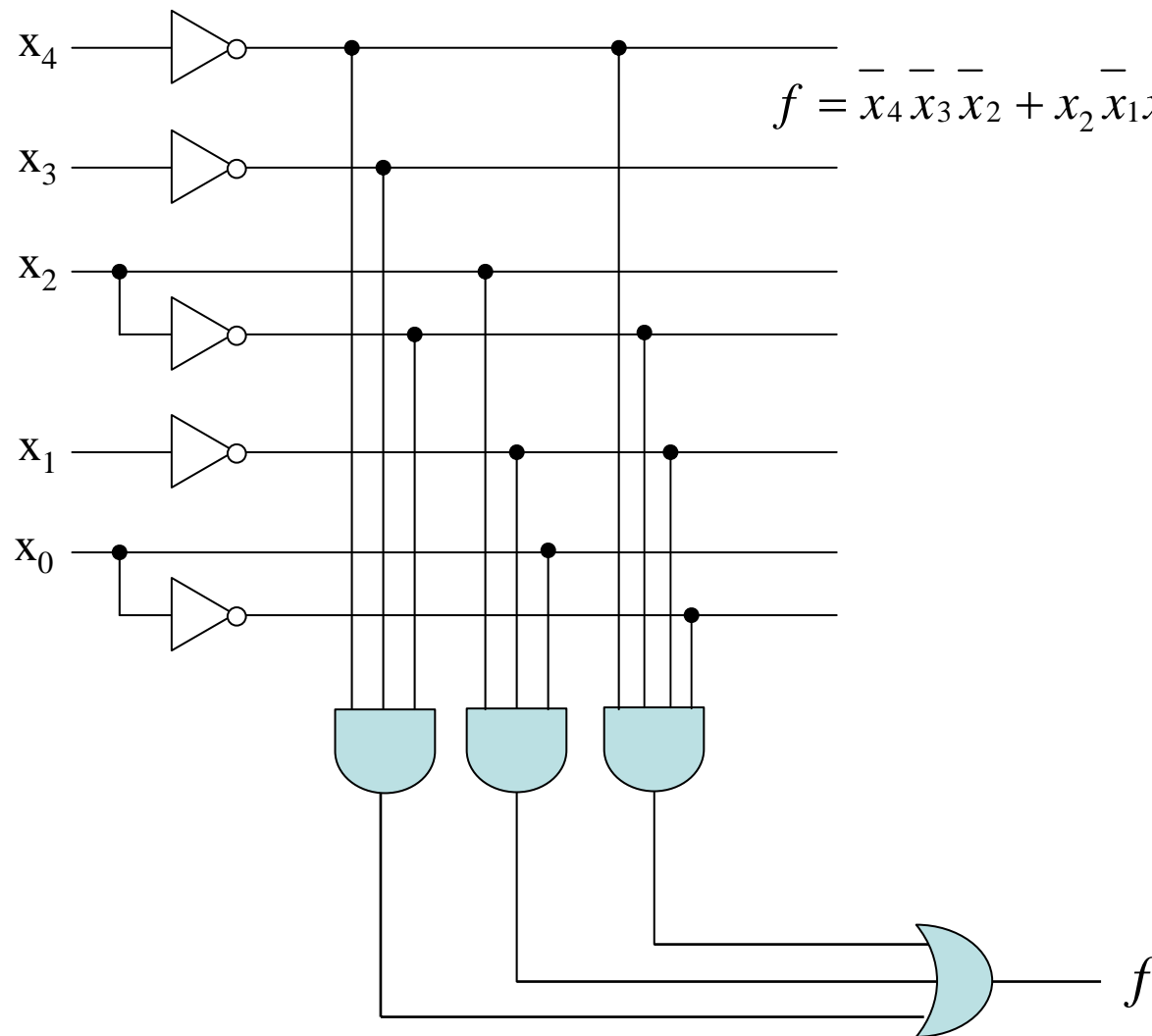
$$x_4 = 0$$

$$x_4 = 1$$

$$f = \overline{x_4} \overline{x_3} \overline{x_2} + x_2 \overline{x_1} x_0 + \overline{x_3} \overline{x_2} \overline{x_1} x_0$$



Quesito 1 – Sintesi a 2 livelli di logica [Soluzione A]





Quesito 4 - 1/3

	T ₁				T ₂				T ₃			
	V	D	Tag	Value	V	D	Tag	Value	V	D	Tag	Value
00	0	-	-	-	1	0	0011	Mem[001100]	1	0	0011	Mem[001100]
	0	-	-	-	0	-	-	-	0	-	-	-
01	0	-	-	-	0	-	-	-	0	-	-	-
	0	-	-	-	0	-	-	-	0	-	-	-
10	1	0	1101	Mem[110110]	1	0	1101	Mem[110110]	1	0	1101	Mem[110110]
	0	-	-	-	0	-	-	-	0	-	-	-
11	0	-	-	-	0	-	-	-	1	0	1100	Mem[110011]
	0	-	-	-	0	-	-	-	0	-	-	-
MISS				MISS				MISS				



Quesito 4 - 2/3

		T ₄				T ₅				T ₆			
		V	D	Tag	Value	V	D	Tag	Value	V	D	Tag	Value
00		1	0	0011	Mem[001100]	1	0	0011	Mem[001100]	1	0	0011	Mem[001100]
		0	-	-	-	1	0	1110	Mem[111000]	1	0	1011	Mem[101100]
01		0	-	-	-	0	-	-	-	0	-	-	-
		0	-	-	-	0	-	-	-	0	-	-	-
10		1	0	1101	Mem[110110]	1	0	1101	Mem[110110]	1	0	1101	Mem[110110]
		0	-	-	-	0	-	-	-	0	-	-	-
11		1	0	1100	Mem[110011]	1	0	1100	Mem[110011]	1	0	1100	Mem[110011]
		0	-	-	-	0	-	-	-	0	-	-	-
		HIT				MISS				MISS			



Quesito 4 - 3/3

	T ₇				T ₈				T ₉			
	V	D	Tag	Value	V	D	Tag	Value	V	D	Tag	Value
00	1	0	0011	Mem[001100]	1	0	0011	Mem[001100]	1	0	0011	Mem[001100]
	1	0	1011	Mem[101100]	1	0	1011	Mem[101100]	1	0	1011	Mem[101100]
01	0	-	-	-	0	-	-	-	0	-	-	-
	0	-	-	-	0	-	-	-	0	-	-	-
10	1	0	1101	Mem[110110]	1	0	1101	Mem[110110]	1	0	1101	Mem[110110]
	0	-	-	-	0	-	-	-	0	-	-	-
11	1	0	1100	Mem[110011]	1	0	1100	Mem[110011]	1	0	1101	Mem[110111]
	1	0	1111	Mem[111111]	1	0	1111	Mem[111111]	1	0	1111	Mem[111111]
MISS				HIT				MISS				



Quesito 4.a – 1/2

	T_9				T_{10}				T_{11}			
	V	D	Tag	Value	V	D	Tag	Value	V	D	Tag	Value
00	1	0	0011	Mem[001100]	1	0	0011	Mem[001100]	1	0	0011	Mem[001100]
	1	0	1011	Mem[101100]	1	0	1011	Mem[101100]	1	0	1011	Mem[101100]
01	0	-	-	-	0	-	-	-	0	-	-	-
	0	-	-	-	0	-	-	-	0	-	-	-
10	1	0	1101	Mem[110110]	1	1	1101	Mem[110110]	1	1	1101	Mem[110110]
	0	-	-	-	0	-	-	-	1	0	1111	Mem[111110]
11	1	0	1101	Mem[110111]	1	0	1101	Mem[110111]	1	0	1101	Mem[110111]
	1	0	1111	Mem[111111]	1	0	1111	Mem[111111]	1	0	1111	Mem[111111]
					HIT				MISS			

Scrittura solo in cache!



Quesito 4.a – 2/2

T_{12}				
	V	D	Tag	Value
00	1	0	0011	Mem[001100]
	1	0	1011	Mem[101100]
01	0	-	-	-
	0	-	-	-
10	1	1	1101	Mem[110110]
	1	0	0001	Mem[000110]
11	1	0	1101	Mem[110111]
	1	0	1111	Mem[111111]
MISS				



Quesito 4.b – 1/2

	T_9				T_{10}				T_{11}			
	V	D	Tag	Value	V	D	Tag	Value	V	D	Tag	Value
00	1	0	0011	Mem[001100]	1	0	0011	Mem[001100]	1	0	0011	Mem[001100]
	1	0	1011	Mem[101100]	1	0	1011	Mem[101100]	1	0	1011	Mem[101100]
01	0	-	-	-	0	-	-	-	0	-	-	-
	0	-	-	-	0	-	-	-	0	-	-	-
10	1	0	1101	Mem[110110]	1	1	1101	Mem[110110]	1	1	1101	Mem[110110]
	0	-	-	-	0	-	-	-	1	0	1111	Mem[111110]
11	1	0	1101	Mem[110111]	1	0	1101	Mem[110111]	1	0	1101	Mem[110111]
	1	0	1111	Mem[111111]	1	0	1111	Mem[111111]	1	0	1111	Mem[111111]
					HIT				MISS			

Scrittura solo in cache!



Quesito 4.b – 2/2

	T ₁₂				T ₁₃				T ₁₄			
	V	D	Tag	Value	V	D	Tag	Value	V	D	Tag	Value
00	1	0	0011	Mem[001100]	1	0	0011	Mem[001100]	1	0	0011	Mem[001100]
	1	0	1011	Mem[101100]	1	0	1011	Mem[101100]	1	0	1011	Mem[101100]
01	0	-	-	-	0	-	-	-	0	-	-	-
	0	-	-	-	0	-	-	-	0	-	-	-
10	1	1	1101	Mem[110110]	1	1	1101	Mem[110110]	1	0	0001	Mem[000110]
	1	0	1111	Mem[111110]	1	0	1111	Mem[111110]	1	0	1111	Mem[111110]
11	1	0	1101	Mem[110111]	1	0	1101	Mem[110111]	1	0	1101	Mem[110111]
	1	0	1111	Mem[111111]	1	0	1111	Mem[111111]	1	0	1111	Mem[111111]
	HIT				HIT				MISS			

Il blocco rimpiazzato è stato modificato [$\leftrightarrow D=1$]; la modifica deve essere propagata in memoria [write back]



Quesito 5 – 2 FF T in cascata [“tipo contatore”] come divisore di frequenza $ck' \Rightarrow ck'/4$

